Abstract

High speed processor

High speed processor having a data processing unit (13) for processing data, a data memory (20) which is connected to the data processing unit via a data bus (10) and can be addressed by the data processing unit (13) via a data memory address bus (18), at least one input interface buffer (9) which is connected to the data bus (10) and has the purpose of buffering input data, at least one output interface buffer (16) which is connected to the data bus (10) and has the purpose of buffering output data, the input interface buffer (9) and the output interface buffer (26) being directly addressable by the data processing unit (13) via an interface address bus (24).

Figure 4